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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/092,158	06/05/1998	SAILESH M. MERCHANT	MERCHANT3333	5736
27964 7	590 08/25/2004		EXAM	INER
HITT GAINES P.C. P.O. BOX 832570			MALDONADO, JULIO J	
RICHARDSON, TX 75083			ART UNIT	PAPER NUMBER
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DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

		Application No.	Applicant(s)			
Office Action Summary		09/092,158	MERCHANT ET AL.			
		Examiner	Art Unit			
		Julio J. Maldonado	2823			
Period fo	The MAILING DATE of this communication or Reply	appears on the cover sheet with	the correspondence address			
THE I - Exter after - If the - If NO - Failu Any r	ORTENED STATUTORY PERIOD FOR RIMAILING DATE OF THIS COMMUNICATION Is sions of time may be available under the provisions of 37 CF SIX (6) MONTHS from the mailing date of this communication period for reply specified above is less than thirty (30) days, period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by seply received by the Office later than three months after the red patent term adjustment. See 37 CFR 1.704(b).	ON. R 1.136(a). In no event, however, may a replyon. n. a reply within the statutory minimum of thirty (3 eriod will apply and will expire SIX (6) MONTH statute, cause the application to become ABAN	y be timely filed 30) days will be considered timely. S from the mailing date of this communication. DONED (35 U.S.C. § 133).			
Status						
1)⊠	1)⊠ Responsive to communication(s) filed on 14 June 2004.					
2a) <u></u> ☐						
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Dispositi	on of Claims					
4)⊠ 5)□ 6)⊠ 7)□	 Claim(s) 1,4-12 and 15-24 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. Claim(s) is/are allowed. Claim(s) 1,4-12 and 15-24 is/are rejected. Claim(s) is/are objected to. 					
Applicati	on Papers					
9)□ .	9) The specification is objected to by the Examiner.					
10)[10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.					
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.					
Priority u	nder 35 U.S.C. § 119					
a)[Acknowledgment is made of a claim for formula All b) Some * c) None of: 1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the application from the International Butter the attached detailed Office action for a	nents have been received. nents have been received in App priority documents have been re reau (PCT Rule 17.2(a)).	lication No ceived in this National Stage			
Attachment	(s)					
	e of References Cited (PTO-892)	4) Interview Sum				
3) 🔲 Inforn	e of Draftsperson's Patent Drawing Review (PTO-948 nation Disclosure Statement(s) (PTO-1449 or PTO/SE No(s)/Mail Date		fail Date mal Patent Application (PTO-152)			

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DETAILED ACTION

- 1. The rejection as set forth in paper mailed on 02/12/2004 is withdrawn in view of applicants' arguments on claims 4 and 15, filed on 06/14/2004.
- 2. A new rejection is included in this action.
- 3. Claims 1, 4-12 and 15-24 are pending in the application.

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 1, 5-12, 16, 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. 5,591,671) in view of Bai et al. (U.S. 5,714,418) and Teo (U.S. 5,970,374).

In reference to claims 1, 7, 12, 18 and 24, Kim et al. (Figs.2-4) in a related method to form an interconnect layer teach the steps of forming a contact opening (25) in a dielectric layer (24) on a semiconductor substrate (21, 24), said contact opening (25) electrically contacting an active device; depositing by physical vapor deposition (PVD) a barrier layer (26, 27) in said contact opening (25) and on at least a portion of said semiconductor substrate (21, 24), said barrier layer deposition step includes depositing titanium layer (26) and depositing titanium nitride layer (27) on said titanium layer (26); depositing a contact metal (28) on said barrier layer (26, 27) within said contact opening (25); removing a substantial portion of said contact metal (28) and said

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barrier layer (26, 27) from said semiconductor substrate (21, 24) to form a contact plug within said contact opening (25) (column 5, lines 24 – 39); and subjecting said contact plug to a heating treatment, changing the crystalline structure (i.e., annealing) of the barrier layer (26, 27) to reduce ohmic contact (column 4, line 27 – column 6, line 56).

Kim et al. fail to teach extending the plug to an uppermost surface of said substrate. However, Bai et al. (Figs.4C-4D) in a related method to form planarized interconnects in a semiconductor device teach the steps of removing a substantial portion a contact metal (44) and a barrier layer (42, 43) from a semiconductor substrate (40, 41) to form a contact plug within a contact opening (47), said plug extending to an uppermost surface of said substrate (40, 41) (column 9, lines 12-25). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Kim et al. and Bai et al. to enable the removing step of Kim et al. to be performed according to the teachings of Bai et al. because this would isolate the interconnect layer within the trench (column 9, lines 18 - 20) and because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed removing step of Kim et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Kim et al. and Bai et al. fail to teach wherein said heat treatment is a rapid thermal anneal process performed from about 5 to 60 seconds, at a temperature from about 600°C to about 750°C. However, Teo in a related method to form interconnects teaches the step of using rapid thermal annealing to a Ti/TiN layer

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at a temperature of about 670°C for about 30 seconds (column 3, lines 30 – 35 and column 4, lines 17-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a RTA process as taught by Teo and in the combination of Kim et al. and Bai et al., since this improves the adhesion of the barrier layer in the contact opening (column 4, lines 17-25).

Still the combined teachings of Kim et al., Bai et al. and Teo fail to teach performing the thermal anneal from 5 to 60 seconds at a temperature form about 600°C to 750°C. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the annealing specifications disclosed in the combined teachings of Kim et al., Bai et al. and Teo to arrive at the claimed invention.

In reference to claims 5, 6, 16 and 17, the combined teachings of Kim et al., Bai et al. and Teo teach depositing a tungsten contact by chemical vapor deposition (Kim et al., column 4, line 57 – column 5, line 4).

In reference to claims 8, 9, 19, 20 and 23, Kim et al. in combination with Bai et al. and Teo teach depositing a barrier layer including forming a thickness of said barrier layer ranging from about 90 nm to about 290 nm within said contact opening having a design width below 1µ and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater (Kim et al., column 4, lines 38-44). Kim et al. in combination with Bai et al. fail to teach the thickness of said barrier layer from about 5 nm to about 20 nm and having 5% to about 20% of field area thickness

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within said contact opening. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In reference to claims 10, 11, 21 and 22, Kim et al. in combination with Bai et al. and Teo teach removing a substantial portion including removing said contact metal and said barrier layer from said field area thickness by chemical mechanical polishing processes (Kim et al., column 5, lines 62-67 and Bai et al., lines column 9, lines 12-24).

6. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. ('671) in view of Bai et al. ('418) and Teo ('374) as applied to claims 1, 5-12, 16, 17-24 above, and further in view of the applicants admitted prior art in the instant application.

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Kim et al. in combination with Bai et al. and Teo teach depositing a barrier layer in a contact opening in a dielectric layer, but fail to show the contact opening with an aspect ratio ranging from about 3:1 to about 5:1. However, the prior art teaches forming openings having aspect ratios from about 3:1 to about 5:1 (page 2, lines 1-6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify aspect ratios of about 3:1 to about 5:1 as taught by the prior art and include it in the combination of Kim et al. and Bai et al., since this fulfill the need for forming smaller devices (page 1, line14 - page 2, line 6).

Response to Arguments

7. Applicant's arguments filed 02/12/2004 have been fully considered but they are not persuasive.

Applicants argue, "... one skilled in the art would not be motivated to incorporate Bai's removing method into Kim's removing step in the manner suggested by the Examiner, because there is no suggestion or motivation in the references themselves to support their combination, and there is not a reasonable expectation of success... Bai's method of removing is not suitable for use in Kim process flow, because it would expose portions of Kim's barrier layer to oxidation during thermal annealing, which Kim expressly wishes to avoid...". In response to applicants' arguments, Kim et al. teach an embodiment of the invention (not illustrated), wherein after forming the metal plug, patterning the plug along with the barrier and low-ohmic layer, followed by forming an optional oxidation barrier layer if the metal plug is susceptible to oxidation (column 5, lines 24 – 42). Furthermore, Kim et al. is silent to the form of this pattern. Thus

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combining Kim et al. and Bai et al., it is demonstrated that a plug with an "uppermorst surface extending to the surface of the substrate" as recited in claim 1, can be obtained. Furtherstill, Bai et al. show that said patterning is known in the art (Bai et al., Fig.2). Although an oxidized surface of the metal plug would not be expected if a metal not susceptible to oxidation is employed and the barrier is omitted.

Also, Applicants argue, "... Teo is not properly combinable with the combination of Kim and of Bai...". In response to applicants' arguments, Kim et al. teach that after forming a metal plug, the device is heated at a temperature of above 450°C, but preferably from 500°C-550°C (Kim et al., column 4, lines 57 – 64). Kim et al. is silent as to the type of heating process used, the duration of said heating process and the temperatures used on said heating process, although is open to perform said heating process at temperatures above 450°C as mentioned above. Taking this into consideration, Teo teaches that by using rapid thermal annealing on a Ti/TiN layer at a temperature of about 670°C for about 30 seconds (column 3, lines 30 – 35 and column 4, lines 17-25), the adhesion of said barrier layer in the contact opening will be improved (column 4, lines 17-25). Therefore, Kim et al. is open to perform the heating process described in Teo, and furthermore because of the adhesion improvement as mentioned above. Furthermore, although Kim et al. teach adverse effects if said heating process is performed at temperatures of above 500°C (column 2, lines 12 – 20), Kim et al. teach that said adverse effects occur in an oxygen-containing atmosphere, to which Kim et al. teach performing said heating process in a nitrogen or argon containing atmosphere

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(Kim et al., column 5, lines 9 - 14). Furtherstill, the claimed invention is silent to any particularities regarding the atmospheric conditions used in the annealing process.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number

is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this

group is 703-872-9306 for before final submissions, 703-872-9306 for after final

submissions and the customer service number for group 2800 is (703) 306-3329.

Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado Patent Examiner Art Unit 2823

Julio J. Maldonado August 18, 2004

> George Fourson Primary Examiner